WHAT IS CLAIMED IS:

1. A level detection circuit that detects a level change of a input value, comprising:

a multiplication unit which multiplies the input value by a value;

an integration unit which integrates a result of multiplication by the multiplication unit; and

a comparison unit which compares a result of integration by the integration unit with the input value, and detects a level change of the input value.

2. A level detection circuit according to claim 1, wherein the multiplication unit multiplies the input value by $1/a - b/c$, wherein a, b, and c are arbitrary numbers, and

the integration unit includes an adder unit, and an arithmetic unit which multiplies a result of addition by the adder unit by $1 - 1/a$, the adder unit adding a result of multiplication by the multiplication unit and a result of computation by the arithmetic unit.

3. A level detection circuit according to claim 2, wherein the input value, a, b, and c are binary numbers, and the level detection circuit further comprises:

a first bit adjustment unit which adjusts the number of bits of the input value input to the multiplication unit; and

a second bit adjustment unit which adjusts the number of bits of the result of integration such that the number of bits of the result of integration equals the number of bits of the input value when the result of integration and the input value are compared by the comparison unit.

4. A phase change detection circuit that detects a phase change of an input signal, comprising:

a sine wave generating circuit which generates, from the input signal, a reference sine wave having the same period as the input signal;

a first integration unit which multiplies the input signal by the reference sine wave, integrates a result of the multiplication, and provides a first integration result;

a multiplication unit which multiplies the first integration result by a value, and provides a multiplication result;

a second integration unit which integrates the multiplication result, and provides a second integration result; and

a comparison unit which detects a level change of the first integration result as a phase change of the input signal by comparing the first integration result and the second integration result.

5. A phase change detection circuit according to claim 4, wherein the multiplication unit multiplies

the input value by 1/a - b/c where a, b, and c are arbitrary numbers,

the second integration unit includes an adder unit, and an arithmetic unit which multiplies a result of addition by the adder unit by 1 - 1/a, and

the adder unit adds the multiplication result provided by the multiplication unit and a result of computation by the arithmetic unit.

6. A phase change detection circuit according to claim 5, wherein the input value, a, b, and c are binary numbers, and the phase change detection circuit further comprises:

a first bit adjustment unit which adjusts the number of bits of the input value input to the multiplication unit; and

a second bit adjustment unit which adjusts the number of bits of the second integration result such that the number of bits of the second integration result equals the number of bits of the input value when the second integration result and the input value are compared by the comparison unit.

7. An optical disk comprising:

a wobble signal generating unit which generates a wobble signal from reflected light from a track on an optical disk on which a wobble, modulated using an address signal, is formed;

a sine wave generating unit which generates,

from the wobble signal, a reference sine wave having the same period as the wobble signal;

a first integration unit which multiplies the wobble signal by the reference sine wave, integrates a result of multiplication, and provides a first integration result;

a level detection unit which detects a level change of the first integration result as a phase change of the wobble signal; and

an address extraction unit which extracts the address signal from the wobble signal in response to detection of the phase change,

wherein the level detection unit comprises:

a multiplication unit which multiplies the first integration result by a value, and provides a multiplication result;

a second integration unit which integrates the multiplication result, and provides a second integration result; and

a comparison unit which compares the first integration result and the second integration result, and detects a signal level change of the first integration result.

8. An optical disk according to claim 7, wherein the multiplication unit multiplies the input value by 1/a - b/c, wherein a, b, and c are arbitrary numbers, and

the integration unit includes an adder unit, and an arithmetic unit which multiplies a result of addition by the adder unit by 1 - 1/a, the adder unit adding the multiplication result provided by the multiplication unit and a result of computation by the arithmetic unit.

9. An optical disk apparatus according to claim 8, wherein the input value, a, b, and c are binary numbers, and the phase change detection circuit further comprises:

a first bit adjustment unit which adjusts the number of bits of the input value input to the multiplication unit; and

a second bit adjustment unit which adjusts the number of bits of the second integration result such that the number of bits of the second integration result equals the number of bits of the input value when the second integration result and the input value are compared by the comparison unit.